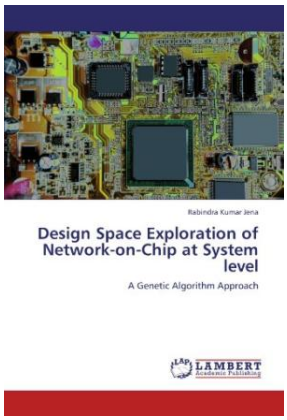
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DESIGN SPACE EXPLORATION OF NETWORK-ON-CHIP AT SYSTEM LEVEL



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